a first differential amplifier circuit including a differential input portion comprising a pair of MOS transistors of a first conductivity type;

a second differential amplifier circuit including a differential input portion comprising a pair of MOS transistors of a second conductivity type; and

an oscillator having a first signal and a second signal from first and second terminals, respectively, each of said first and second signals having an operating point potential that is different than the other and said first signal being input to both said first and second differential amplifier circuits and said second signal being input to both said first and second differential amplifier circuits to generate differential amplification outputs based on said first and second signals;

wherein the differential amplification outputs of said first and second differential amplification circuits are combined to provide an output.

8. (Amended) An oscillation circuit, comprising:

an oscillator having a first signal and a second signal from first and second terminals, respectively, each of said first and second signals having an operating point potential that is different than the other and said first signal being input to both said first and second differential amplifier circuits and said second signal being input to both said first and second differential amplifier circuits to generate differential amplification outputs based on said first and second signals;

a first MOS transistor of a first conductivity type having a source, a drain and a gate, and receiving said first signal at the gate thereof;

a second MOS transistor of the first conductivity type having a source, a drain and a gate, and receiving said second signal at the gate thereof;

a first current mirror circuit comprising a third and a fourth MOS transistors of a second conductivity type each having a source, a drain and a gate, the drains of said third and fourth MOS transistor being connected to the drains of said first and second MOS transistors, respectively, the gates of the third and fourth MOS transistors connected to each other and the gate and drain of said third MOS transistor;

a fifth MOS transistor of the second conductivity type having a source, a drain and a gate, and receiving the first signal at the gate thereof;

a sixth MOS transistor of the second conductivity type having a source, a drain and a gate, and receiving the second signal at the gate thereof;

a second current mirror circuit comprising a seventh and an eighth MOS transistors of the first conductivity type each having a source, a drain and a gate, the drains of said seventh and eighth MOS transistors being connected to the drains of said fifth and sixth MOS transistors, respectively, the gates of the seventh and eighth MOS transistors being connected to each other and the gate and drain of said seventh MOS transistor being connected; and

an output buffer circuit for generating an output signal based on a signal generated at the drain of said fourth MOS transistor and a signal generated at the drain of said eighth MOS transistor.